

WHAT IS CLAIMED IS:

- 1           1.    An integrated circuit fabrication process, the process comprising  
2 the steps of:  
3                patterning a transistor gate pattern on a photoresist layer;  
4                curing the transistor gate pattern with an electron beam;  
5                trimming the cured transistor gate pattern; and  
6                transferring the trimmed transistor gate pattern to a layer  
7 disposed below the photoresist layer to form a transistor gate, wherein the  
8 transistor gate includes a width and a length, and a variation of the width  
9 along the length of the transistor gate is reduced due to the curing step.
- 1           2.    The process of claim 1, wherein the photoresist layer is  
2 comprised of a photoresist material typically used for at least one of 248 nm  
3 lithography, 193 nm lithography, and extreme ultraviolet light (EUV)  
4 lithography.
- 1           3.    The process of claim 2, wherein the photoresist layer is comprised  
2 of a photoresist material of a type typically used for 193 nm and 248 nm  
3 lithography and is commercially available.
- 1           4.    The process of claim 1, wherein the final gate transistor width is  
2 in the range of approximately 20-60 nm.
- 1           5.    The process of claim 1, wherein the curing step includes exposing  
2 the transistor gate pattern to the electron beam having a dose in the range of  
3 approximately 100-100000  $\mu\text{C}/\text{cm}^2$ .
- 1           6.    The process of claim 1, wherein the curing step includes exposing  
2 the transistor gate pattern to the electron beam having an accelerating voltage  
3 in the range of approximately 0.5-20 Kv.

1           7. The process of claim 1, wherein the curing step includes changing  
2 at least one of a vertical etch rate, a horizontal etch rate, and a minimum  
3 extension erosion rate associated with the transistor gate pattern.

1           8. A method of forming a transistor having a gate width of less than 70  
2 nm, the method comprising the steps of:

3                   E-beam radiating a gate pattern of a photoresist layer;  
4                   trimming the E-beam eradiated gate pattern of the photoresist  
5 layer; and

6                   etching a polysilicon layer disposed below the photoresist layer  
7 in accordance with the trimmed gate pattern to form a gate of the transistor,  
8 the gate width being less than 70 nm.

1           9. The method of claim 8, wherein the E-beam radiating step uses an  
2 electron beam at a dose in the range of approximately 100-100000  $\mu\text{C}/\text{cm}^2$ .

1           10. The method of claim 9, wherein the electron beam is provided at  
2 an accelerating voltage in the range of approximately 0.5-50 Kv.

1           11. The method of claim 9, wherein a uniformity of the gate width is  
2 4 to 6 nm over 3 nm segment.

1           12. The method of claim 9, wherein the photoresist layer is comprised  
2 of a material selected from a group including acrylate-based polymer,  
3 alicyclic-based polymer, and phenolic-based or polystyrene-based polymer.

1           13. The method of claim 9, wherein the E-beam radiation step includes  
2 affecting at least one of a vertical etch rate, a horizontal etch rate, and a  
3 minimum extension erosion rate associated with the gate pattern of the  
4 photoresist layer.

1           14. The method of claim 9, wherein the E-beam radiation step  
2 achieves an enhancement interim rate for a commercially available resists

3 using lithography processes with either 248 nm and 193 nm wavelength of  
4 light.

1 15. An integrated circuit, comprising:  
2 an isolation region;  
3 a transistor surrounded by the isolation region, wherein the  
4 transistor includes a gate, a critical dimension of the gate being less than  
5 approximately 60 nm, and the gate being defined by an E-beam irradiated  
6 gate feature on a photoresist layer.

1 16. The integrated circuit of claim 15, wherein the E-beam irradiated  
2 gate feature on the photoresist layer is formed by an electron beam exposure.

1 17. The integrated circuit of claim 15, wherein a uniformity of the critical  
2 dimension along a length of the gate is 4 to 6 nm over a 3 nm segment.

1 18. The integrated circuit of claim 15, wherein the photoresist layer  
2 is comprised of a material selected from acrylate-based polymer, alicyclic-  
3 based polymer, and polystyrene and phenolic-based polymer.

1 19. The integrated circuit of claim 18 wherein the critical dimension  
2 is between 20 and 60 nm.

1 20. The integrated circuit of claim 18 wherein uniformity of the  
2 critical dimension along a length of the gate is 4 to 6 more a 3 nm segment.